Evaluating the Impact of Interconnections in Quantum-dot Cellular Automata (QCA)

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Outline

- Motivation
- Design Automation
- Analysis Environment
- Results
- Conclusions
Motivation

Quantum-dot Cellular Automata (QCA)

- Promising nanotechnology based on quantum dots
- Remarkable low energy dissipation
- Several (experimental) physical realizations based on different concepts (Metal islands, nanomagnets, dangling bonds, …)
Motivation

Interconnections

- Challenging routing in QCA
  - QCA is (nearly) planar technology
    - Current state: 1 layer for logic & routing, 1 layer for crossings
    - Outlook: low amount of layers
  - Data flow must follow clocking constraint (clock 1 → clock 2 → clock 3 → …)
  - Only orthogonal routing

- Simple example:
Motivation

Interconnections cont’d

- More complex design

- Interconnections with notable impact on Area, Delay, Energy increase

- Question: What is the actual impact?
Design Automation

Comparison

CMOS Process

- Conceptual Design
- Behavioral Model
- Structural Model
- Electric Model
- Layout

- No Differences

QCA Process

- Conceptual Design
- Behavioral Model
- Structural Model
- QCA Model
- Layout

- Some Differences

Transistors and connections
MOS layers

QCA cells and its positions
Layers of specific material
if a > 0 then
    ergebnis := (a + b/2);
else
    ergebnis := -(a + b/2);
end if;

HDL Description

Netlist

Tile (clock zone) grid

Layout
Design Automation

Gate Library

Routing Elements
- Wire
- Bent wire
- Fanout

Simple Gates
- Inverter
- Majority
- OR

Complex Gates
- NOR
- XOR
Components of energy dissipation of QCA:

- Energy from clock: $E_{clk}$
- Energy from neighboring cell(s): $E_{in}$
- Energy to environment: $E_{env}$
- Energy to neighboring cell(s): $E_{out}$

Dissipated energy: $E_{env} = E_{clk} + E_{in} - E_{out}$

\[
E_{env} = \frac{\hbar}{2} \int \left( \vec{\Gamma} \cdot \vec{\lambda} + |\vec{\Gamma}| \tanh \eta_{th} \right) dt'
\]

QCADesigner-E - Physics simulator including determination of energy dissipation of QCA (https://github.com/FSillIT/QCADesigner-E)
## Characterized Gate library

<table>
<thead>
<tr>
<th>Routing Elements</th>
<th>Area [µm²]</th>
<th>Delay [tiles]</th>
<th>Energy Dissipation [meV]</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Regl. Mode (25 GHz)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>000  ... 111</td>
</tr>
<tr>
<td>Wire</td>
<td>0.01</td>
<td>1</td>
<td>0.09 ... -</td>
</tr>
<tr>
<td>Bent-wire</td>
<td>0.01</td>
<td>1</td>
<td>0.10 ... -</td>
</tr>
<tr>
<td>Fanout</td>
<td>0.01</td>
<td>1</td>
<td>0.12 ... -</td>
</tr>
<tr>
<td>Inverter</td>
<td>0.01</td>
<td>1</td>
<td>0.13 ... -</td>
</tr>
<tr>
<td>Majority</td>
<td>0.01</td>
<td>1</td>
<td>0.15 ... 0.15</td>
</tr>
<tr>
<td>OR</td>
<td>0.01</td>
<td>1</td>
<td>0.18 ... -</td>
</tr>
<tr>
<td>NOR</td>
<td>0.02</td>
<td>2</td>
<td>0.31 ... -</td>
</tr>
<tr>
<td></td>
<td>...</td>
<td>...</td>
<td>...</td>
</tr>
</tbody>
</table>
Analysis Environment

P&R Algorithm

1. Diagonal arrangement of clocking

2. Levelizing of netlist graph

3. Diagonal placement of each level

4. Routing
Analysis Environment

Flow

- **Synthesis:**
  - Synthesis library (*.lib) for QCA gate library
  - Synopsys Design Compiler
  - ABC (AIG, BDD)

- **EFPL Benchmarks**

<table>
<thead>
<tr>
<th>Benchmark name</th>
<th>Inputs</th>
<th>Outputs</th>
<th>AND nodes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Adder (adder)</td>
<td>256</td>
<td>129</td>
<td>1020</td>
</tr>
<tr>
<td>Barrel shifter (barrel)</td>
<td>135</td>
<td>128</td>
<td>3336</td>
</tr>
<tr>
<td>Max (max)</td>
<td>512</td>
<td>130</td>
<td>2865</td>
</tr>
<tr>
<td>Sine (sin)</td>
<td>24</td>
<td>25</td>
<td>5416</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
<td>...</td>
<td>...</td>
</tr>
</tbody>
</table>
Results

Area

![Graph showing area vs. interconnection overhead for different benchmarks]

- AND nodes of initial benchmarks
- Interconnection Overhead vs. Area
- Points represent different benchmarks:
  - AIG
  - BDD
  - Comm

Sill Torres – QCA
Results

Delay

![Graph showing Delay and Interconnection Overhead for AND nodes of initial benchmarks. The graph compares AIG, BDD, and Comm.]
Results

Energy Dissipation

![Graph showing energy dissipation vs. interconnection overhead for AIG, BDD, and Comm benchmarks. The x-axis represents the number of AND nodes of initial benchmarks, ranging from 0 to 6000. The y-axis represents the interconnection overhead, ranging from 0 to 700. Different markers signify AIG, BDD, and Comm benchmarks, with distinct colors for each.](image-url)
Conclusions

- QCA is a promising nanotechnology for low energy applications
- Specific characteristics of QCA design require notable amount of interconnections
- Here: Evaluation of this impact
- Results indicate high impact of Interconnections with consequences on area, delay, energy
- Requirements for future research:
  - Comprehensive synthesis cost model for interconnections
  - New synthesis strategies with emphasis on reduction of interconnections
  - Exploration of new concepts (systolic arrays, logic duplication, …)
Thank you!

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