Exploration of Technology Parameter Values of Integrated Circuits

Rodrigo Fonseca Rocha Soares – UFMG
Frank Sill Torres – DELT/UFMG
Dirk Timmermann – University of Rostock
Focus / Principal idea:

Technology Parameter Exploration of Integrated Circuits

Standard-Cell Characterization Flow for Novel Technologies
Outline

1. Motivation
2. Methodology
3. Results
4. Conclusion
Motivation

Technology Parameters

- Integrated circuit technologies offer two kind of parameters:
  - Design parameters (e.g. transistor width, transistor length)
  - Technology parameters (e.g. doping, oxide thickness)
- Design parameters
  - Constrained
  - Modifiable by circuit designers
- Technology parameters:
  - Constrained
  - Not accessible by circuit designers
  - Can be oriented to consumer applications profiles
    (e.g. High performance / Low-power)
Motivation

Technology Parameter Values

- **Question:** How to chose values for technology parameters?
- **Several constraints:** $I_{on}$ vs. $I_{off}$ currents, area, gain, …
- **Interesting for:**
  - Technology engineers
  - Researchers for novel technologies (CNTFET, SET, …)
- **Common approach:**
  - Analysis using **selected cells** (FO4 configuration)
  - **Sweep** of input parameters (e.g. slope, input value, …)
Motivation

Novel Approach

- Problem: Common solution not accurate enough
- Example: Average CMOS PTM22 gains in relation to CMOS PTM32

Proposal:

- Analysis of technology parameter based on actual designs
Methodology

Presentation

- Principal ideas:
  - Analysis of technology parameters impact using characterized standard cell library and test designs
  - Interactive parametric exploration

- Application of commercial tool(s) for standard cell library characterization
- Technology can be given on Spice, Circuit, or Verilog-A level
- Test designs oriented in future application of selected technology
Methodology

- **Two step flow:**
  - Pre-Setup
  - Technology Parameter Exploration

- Pre-Setup
  - Environment Setup
  - Standard-cell representation

- Technology parameter Exploration
  - Standard-cell characterization
  - Benchmark and analysis
Methodology

Pre-Setup Stage:

- Design of standard cell library with default parameter values
- Extraction of parameters for look-up tables in characterization flow
- Selection of most important technology parameters and its ranges for exploration
Methodology

Technology Parameter Exploration

- Start parameters with default values
- Perform characterization and benchmark with actual designs
- Figure of Merit evaluation and analysis
- Iterate

\[
F(\Phi) = \varphi_1 \left( \sum_{\text{designs}} \frac{P_{\text{dyn},i}(\Phi)}{P_{\text{dyn},i,\text{init}}} \right)^{\gamma_1} + \varphi_2 \left( \sum_{\text{designs}} \frac{P_{\text{leak},i}(\Phi)}{P_{\text{leak},i,\text{init}}} \right)^{\gamma_2} \\
+ \varphi_3 \left( \sum_{\text{designs}} \frac{t_{\text{delay},i}(\Phi)}{t_{\text{delay},i,\text{init}}} \right)^{\gamma_3} + \varphi_4 \left( \sum_{\text{designs}} \frac{A_i(\Phi)}{A_i,\text{init}} \right)^{\gamma_4}
\]
Results

Environment

- Analyzed Technologies:
  - PTM22 and PTM32 (based on Predictive Technology Model - PTM)
  - FINFET10-HP FINFET10LL (based on PTM)
  - CNTFET32 and CNTFET22 (based in Stanford CNFET Model)

- Basic standard cell library (10 cells, different sizes, FlipFlop)

- Test Designs:
  - ISCAS suite: c1908, c2670, c3540, c5315, c7552
  - ITC99 suite: b01, b05

- Tools:
  - Cell library characterization: SiliconSmart (Synopsys)
  - Simulation: Virtuoso Analog Design Environment (Cadence)
Results

Technology Comparison – Delay ($t_{\text{delay}}$)

- Versus results for PTM32

![Bar chart showing technology comparison for delay ($t_{\text{delay}}$) vs. $t_{\text{delay}}$@PTM32](chart.png)
Results

Technology Comparison - Power Delay Product (PDP)

- Versus results for PTM32
Results

Technology Comparison – Leakage ($P_{\text{leak}}$)

- Versus results for PTM32
Results

Technology Comparison

- Comparison of relation to PTM32 of FO4 analysis and proposed flow
Results

Parameter Exploration

- Exemplary parameter exploration on CNTFET22 technology
- **Key parameter: tube diameter** (high impact on ON/OFF current)
- **Note:**
  - Number of tubes ($N_{tubes}$): changes
    \[ N_{tubes} = \frac{W_{gate}}{Pitch} - 1 \]
  - Distance between tubes (pitch): constant
  - Channel length ($L_{ch}$): constant
Results

Parameter Exploration

- Results for delay in comparison to standard diameter ($d_{\text{CNT}} = 2\text{nm}$)
Results

Parameter Exploration

- Results for dynamic power consumption ($P_{dyn}$) in comparison to standard diameter ($d_{CNT} = 2\,\text{nm}$)
Results

Parameter Exploration

- Results for leakage in comparison to standard diameter
Results

Parameter Exploration

- Figure of Merit with weights $\phi = 1$, $\gamma = 1$, $\gamma_{\text{leak}} = 1.5$
Conclusion

- New flow for exploration of technologies parameters
- Proposal of Figure of Merit for evaluation of technology parameter set
- Approach based on actual designs
- Increased the quality of predictions by up to 46%
- Applied successfully in CNTFET based technology
Thank you!

OptMA$\text{lab}$ / ART
www.asic-reliability.com
EXTRA CNFET

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Typical Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$W_{\text{gate}}$</td>
<td>Gate width</td>
<td>3a</td>
</tr>
<tr>
<td>$L_{\text{ch}}$</td>
<td>Channel length</td>
<td>2a</td>
</tr>
<tr>
<td>$L_{\text{ss}}$</td>
<td>Doped CNT source-side extension region length</td>
<td>2a</td>
</tr>
<tr>
<td>$L_{\text{dd}}$</td>
<td>Doped CNT drain-side extension region length</td>
<td>2a</td>
</tr>
<tr>
<td>$N_{\text{tub}}$</td>
<td>Number of nanotubes in a device</td>
<td>$(W_{\text{gate}}/\text{Pitch})-1$</td>
</tr>
</tbody>
</table>

**Feature size independent**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Typical Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$d_{\text{CNT}}$</td>
<td>Tubes diameter</td>
<td>1.5 nm</td>
</tr>
<tr>
<td>Pitch</td>
<td>Distance between the centers of two adjacent CNTs within the same device</td>
<td>4 nm</td>
</tr>
<tr>
<td>Distance</td>
<td>Distance between the corners of two adjacent CNTs</td>
<td>2.5 nm</td>
</tr>
<tr>
<td>Tubes density</td>
<td>Tubes density in the device</td>
<td>250 CNT/µm</td>
</tr>
<tr>
<td>$T_{\text{ox}}$</td>
<td>Thickness of high-k top gate dielectric material</td>
<td>4 nm</td>
</tr>
<tr>
<td>$L_{\text{eff}}$</td>
<td>Mean free path in the intrinsic CNT channel region due to non-ideal elastic scattering.</td>
<td>200 nm</td>
</tr>
<tr>
<td>$C_{\text{sub}}$</td>
<td>Coupling capacitance between channel region and substrate</td>
<td>200 nF</td>
</tr>
<tr>
<td>$E_{\text{F}}$</td>
<td>The Fermi level of the doped S/D nanotube.</td>
<td>0.6 eV</td>
</tr>
</tbody>
</table>
## EXTRA FINFET

<table>
<thead>
<tr>
<th>Parameter</th>
<th>FINFET10-HP</th>
<th>FINFET10-LL</th>
</tr>
</thead>
<tbody>
<tr>
<td>L_{ch}</td>
<td>14 nm</td>
<td>14 nm</td>
</tr>
<tr>
<td>P/N*</td>
<td>1x1</td>
<td>1x1</td>
</tr>
<tr>
<td>V_{DD}</td>
<td>0.75 V</td>
<td>0.75 V</td>
</tr>
<tr>
<td>Fin height</td>
<td>21 nm</td>
<td>21 nm</td>
</tr>
<tr>
<td>Fin width</td>
<td>8 nm</td>
<td>8 nm</td>
</tr>
<tr>
<td>EOT</td>
<td>0.68 nm</td>
<td>0.88 nm</td>
</tr>
<tr>
<td>ETA0</td>
<td>0.6778</td>
<td>0.4079</td>
</tr>
</tbody>
</table>
# EXTRA BULK

<table>
<thead>
<tr>
<th>Parameter</th>
<th>PTM32</th>
<th>PTM22</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_{ch}$</td>
<td>32 nm</td>
<td>22 nm</td>
</tr>
<tr>
<td>$W_{min}$</td>
<td>64 nm</td>
<td>44 nm</td>
</tr>
<tr>
<td>$V_{DD}$</td>
<td>1.0V</td>
<td>0.9V</td>
</tr>
</tbody>
</table>

![Diagram of a transistor](image)

- **Gate**
- **Drain**
- **Source**
- **Substrate**
- **Oxide**